

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	3	"7010060".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L3	4925	375/376	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L4	713	((frequency near2 detector) with digital) and (pll or (phase adj locked adj loop)) and vco	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L5	154	L4 and L3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L6	2	10/746434	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L7	2	"6970046".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L8	40	varactor with capacitor and pll and ((frequency adj detector) with digital)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59

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L9	167	((frequency near2 detector) with digital) same (pll or (phase adj locked adj loop)) same vco	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 18:01
L10	47	L9 and L3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L11	64	((frequency near2 detector) with digital) with (pll or (phase adj locked adj loop)) with vco	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L12	2	"4580107".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L13	2	"5,727,038".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L14	0	("7173957").URPN.	USPAT	OR	ON	2007/10/10 17:59
L15	1559	331/11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L16	1	"10/796331"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59

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L17	201	varactor with capacitor and pll and (frequency adj detector)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L18	1015	varactor with capacitor and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L19	1	"10/396118"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L20	2	"5,258,933".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L21	167	((frequency near2 detector) with digital) same (pll or (phase adj locked adj loop)) same vco	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L22	28	L15 and L21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L23	617	((frequency near2 detector) with digital) and pll and vco	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59

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L24	2	"7173957".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L25	13	((frequency near2 detector) with digital) and analog adj loop and digital adj loop and (pll or (phase adj locked adj loop)) and vco	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L26	3	L22 and varactor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L27	28	("4651154" "4701934" "4785463" "5222245" "5365447" "5402347" "5420593" "5535237" "5535278" "5592173" "5594453" "5629708" "5650785" "5663734" "5703597" "5708439" "5781156" "5798732" "5831574" "5841396" "5854605" "5874914" "5884214" "5897605" "5901171" "5943363" "6160858" "6888879").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/10/10 17:59
L28	2	"6094101".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L29	2	"7038497".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L30	1	10/531132	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59

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L31	2	"7157942".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L32	21	L11 and L3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 17:59
L33	2	"4554672".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 18:04
L34	2	"5142246".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 18:06
L35	2	"5714911".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 18:06
L36	2	"6078634".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 18:51
L37	2	"6285219".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 19:34

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L38	2	"7038507".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 19:35
L39	2	"6970046".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 19:36
L40	2	"6683930".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 19:40
L41	2	"6366174".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 19:40
L42	2	"6310521".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/10 19:41

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Phase and frequency **variable oscillator** - Patent 4554672

(c) a **first control input** for accepting a frequency control signal (. 3 is a block diagram of the phase and frequency **variable oscillator** of the ...

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Quadrature oscillator having amplitude control means based on a ...

... and a **first control input** for receiving the control signal, 2 is referred to as a voltage-controllable state-**variable oscillator**. ...

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Oscillators inventions 200707

The load device is configured to provide a **variable oscillator** output based on a The circuit includes an oscillator having a **first control input**, ...

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Multi-loop controlled VCO

... of said oscillator in a first range by producing a **first control input**; and A PLL system having a **variable oscillator** and apparatus for generating ...

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Phase and frequency **variable oscillator**

(c) a **first control input** for accepting a frequency control signal (. ... the output of said phase and frequency **variable oscillator** for modulating a ...

[www.devileye.net/patents/wheelchair_accessory_stand/](http://www.devileye.net/patents/wheelchair_accessory_stand/phase_frequency_variable_oscillator.html)

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The analog loop includes an analog phase **frequency detector** (PFD) and of analog

phase detector 13 is couple to the **first control input** 11a of VCO 11 ...

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[PDF] A MULTI-LEVEL PHASE/FREQUENCY DETECTOR FOR CLOCK AND DATA RECOVERY ...

the critical parts of a CDR. A bang-bang **phase detector** is suitable for. low-power high-bit-rate operation, but a separate **frequency detector** ...

ieeexplore.ieee.org/iel5/10384/33117/01557056.pdf?arnumber=1557056 - Similar pages

[PDF] A Simple Precharged Cmos Phase Frequency Detector - Solid-State ...

If the **phase detector** is used only as a **phase detector**, i.e., not. as a **frequency detector**, the circuit in Fig. 3(a) can be used as ...

ieeexplore.ieee.org/iel3/4/14352/00658634.pdf?arnumber=658634 - Similar pages

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Phase-locked loop (PLL) circuit containing a frequency detector ...

A conventional PLL circuit, having a sampled **phase detector**, a filter and a voltage-controlled oscillator (**VCO**), is modified to include a **frequency detector** ...

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Phase-locked loop (PLL) circuit containing a biased phase detector ...

1, includes a phase and **frequency detector** 110, a **phase detector** 120, a switch 125, a low pass filter 130 and a voltage-controlled oscillator (**VCO**) 140. ...

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Digital phase/frequency detector, and clock generator and data ...

The circuit 10 comprises an **VCO** 12, a divider 14, a frequency difference detector (FDD) 16, a **phase detector** (PD) 18, a phase-frequency detector (PFD) 20, ...

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Linearized digital phase and frequency detector - Patent 4378509

Frequency and **phase detector** 10 (as illustrated in FIG. ... **VCO** are identical in phase and frequency, e.g. when the phase-locked loop is locked. ...

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8.7 **Phase Detector** Design The **phase detector** produces an output signal that is ... The most commonly used **phase detector** is a phase-frequency detector. ...

books.google.com/books?isbn=0849315646...

Phase / frequency detector types | Comp.DSP | DSPRelated.com

Anyway, I've seen several **phase-detector/frequency-detector** circuits and ... are the signals called 'from **VCO** divided by N' and 'from reference frequency'.) ...

www.dsprelated.com/showmessage/22432/1.php - 30k - Cached - Similar pages

Phase-Lock Loop Applications Using the MAX9382 - Maxim/Dallas

The MAX9382 is a phase **frequency detector** which eliminates Phase-Locked Loop (PLL) dead band ... K_1 = **phase detector** transfer gain K_0 = **VCO** transfer gain ...

www.maxim-ic.com/appnotes.cfm/an_pk/1130 - 32k - Cached - Similar pages

[PDF] ADF4002 Phase Detector/Frequency Synthesizer Data Sheet (Rev. A)

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digital phase **frequency detector** (PFD), a precision charge is 3 V, it can. be set to 5.5

http://www.google.com/search?hl=en&rls=GGLD%2CGGLD%3A2004-30%2CGGLD%3... 10/10/07

V and used to drive a VCO with a tuning range of up to 5 V. ...

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Frequency/phase locked loop clock synthesizer using an all digital ...

The analog loop includes an analog phase **frequency detector** (PFD) and charge pump, ...

(VCO), having a **first control** input 11a and **second control** input 11b. ...

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Frequency synthesizer having PLL with an analog phase detector ...

A high frequency, tunable voltage controlled oscillator (VCO) 10 generates ... The phase/frequency detector 18 also receives a reference input signal from a ...
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Self-aligned clock recovery circuit with proportional phase ...

By contrast, the sawtooth phase detector lends itself very well to the addition of a frequency detector. Referring to FIG. 5, if the VCO clock frequency is ...
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an auxiliary digital frequency detector having an output terminal coupled In addition, the PLL may include a voltage controlled oscillator (VCO) having ...
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Digital phase/frequency detector, and clock generator and data ...

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Analog Phase Detector On GlobalSpec

Building blocks of the phase-locked-loop (PLL) circuit to be discussed include an analog phase detector, a temperature-compensated VCO (voltage-controlled ...
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HIGH SPEED CMOS LOGIC PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR ...
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but the most prevalent phase-frequency detector has a charge pump output. ... added to increase the dynamic range of the tuning voltage supplied to the VCO. ...
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Analog mixer • Digital 3 state Phase Frequency Detector • Charge pump circuit ... VCO act as a low pass filter to the control voltage signal ...
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3) Digital phase-frequency detector (CD4046 or MC4044 type). The main advantage of the analog phase detector is its ability to recover a signal from a low ...
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Phase-locked loop - Wikipedia, the free encyclopedia

The **analog phase detector** takes the form of an ideal frequency mixer. ... lock even when it is off frequency and is known as a Phase **Frequency Detector**. ...

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Digital phase-locked loop - US Patent 6970046

... and a **digital frequency detector** provided separately therefrom are used. 8 digitally simulates the behavior of an "ideal" **analog phase detector**. ...

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Digital phase/frequency detector, and clock generator and data ...

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Digital phase-locked loop

5642081, FMCW **VCO** closed... 4583054, Frequency time sta. phase detector and a **digital frequency detector** provided separately therefrom are used. ...

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Digital phase-locked loop

6707342, Multiple-**VCO** tuning. 6714056, Frequency division. phase detector and a **digital frequency detector** provided separately therefrom are used. ...

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Digital phase-locked loop

... which compares the output clock of a voltage-controlled oscillator (**VCO**) ... and a **digital frequency detector** provided separately therefrom are used. ...

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Meltzer, David / Blum, Gregory, UNITED STATES PATENT AND TRADEMARK OFFICE
PRE-GRANT PUBLICATION, Nov 2004

patno:US20040223575

...signals from **analog phase detector** 13 and **digital frequency difference detector** 15 are coupled...inputs of **VCO** 11, respectively...signal of **analog phase detector** 13 is couple...and back to **analog phase detector** 13. The present...path from **digital frequency difference detector** to **VCO** 11 and back...

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VCO AND "analog phase detector" AND "digital frequer

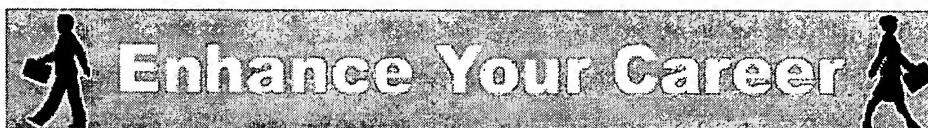
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- ☐ 1. [FREQUENCY/PHASE-LOCKED LOOP CLOCK SYNTHESIZER USING FULL DIGITAL FREQUENCY DETECTOR AND ANALOG PHASE DETECTOR](#)
MELTZER, DAVID / BLUM, GREGORY (SEIKO EPSON CORP), PATENT ABSTRACTS OF JAPAN, Nov 2004
 patno:JP2004312726
 ...using a full **digital frequency detector** and an **analog phase detector**. SOLUTION: A...process controls a **VCO** using a double...there is the full **digital frequency detector** that controls...there is the **analog phase detector** with a charge...
Full text available at patent office. For more in-depth searching go to LexisNexis™
[view all 7 results from Patent Offices](#)
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- ☐ 2. [Frequency/phase locked loop clock synthesizer using an all digital frequency detector and an analog phase detector](#)
Meltzer, David / Blum, Gregory, UNITED STATES PATENT AND TRADEMARK OFFICE PRE-GRANT PUBLICATION, Nov 2004
 patno:US20040223575
 ...design of **VCO** 11 to allow...includes the all **digital frequency detector** 15, which...frequency of **VCO** 11 and thereby...low gain, **analog phase detector**/charge pump...closes the **analog phase detector** loop. This...including the **VCO** modulation...interval for the **digital frequency detector**, i.e. the...
Full text available at patent office. For more in-depth searching go to LexisNexis™
[view all 7 results from Patent Offices](#)
[similar results](#)
- ☐ 3. [Digital phase/frequency detector, and clock generator and data recovery PLL containing the same](#)
Dalmia, Kamal (Cypress Semiconductor Corp.), UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Jan 2004
 patno:US6683930
 ...detector and the **digital frequency detector**, in one example...108 and a **VCO** block (or...implements an **analog phase detector** 62 and a **digital frequency detector** 64. The circuit...summing). The **analog phase detector** 62 is not...
Full text available at patent office. For more in-depth searching go to LexisNexis™
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- ☐ 4. [Method and apparatus for providing a clock generation circuit for digitally controlled frequency or spread spectrum clocking](#)

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Al

F

Berry, John B. / Booth, James R. / Hardin, Keith B. / Richey, John P. (Lexmark International, Inc.), UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED

PATENT, Apr 2002

patno:US6366174

...applied to a voltage controlled oscillator (**VCO**) 40, which produces a high frequency clock...signal at 42. The output frequency at 42 from **VCO** 40 is optionally provided to a divider circuit...used if the output frequency 42 produced by **VCO** 40 is much larger than desired for the output...

Full text available at patent office. For more in-depth searching go to  LexisNexis™

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☐ **5. Reference-free clock generation and data recovery PLL**

Dalmia, Kamal (Cypress Semiconductor Corp.), UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Oct 2001

patno:US6310521

...112 and an **VCO** block (or...detector and a **digital frequency detector**, respectively...implements an **analog phase detector** 62 and a **digital frequency detector** 64. The circuit...summing). The **analog phase detector** 62 is not...

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☐ **6. Reference-free clock generator and data recovery PLL**

Dalmia, Kamal / Agarwal, Anil (Cypress Semiconductor Corp.), UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Oct 2001

patno:US6307413

...half rate **VCO** 12. Referring...implements an **analog phase detector** 62 and a **digital frequency detector** 64. The circuit...summing). The **analog phase detector** 62 is not...diagram of the **VCO** of FIG. 4...comprises a **digital frequency detector**. 4. The apparatus...

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☐ **7. METHOD AND APPARATUS FOR PROVIDING A CLOCK GENERATION CIRCUIT FOR DIGITALLY CONTROLLED FREQUENCY OR SPREAD SPECTRUM CLOCKING**

BERRY, John B. / BOOTH, James R. / HARDIN, Keith B. / RICHEY, John P. (LEXMARK INTERNATIONAL, INC.), PATENT COOPERATION TREATY APPLICATION, Aug 2001

patno:WO0163768

...negative error. This phase detector is an **analog phase detector**, in which the maximum positive error...sine wave that is used to drive an **analog phase detector** of the Phase Locked Loop circuit...the voltage controlled oscillator (**VCO**) also can be optionally divided to...

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...**fast**...

VCO AND "analog phase detector" AND "digital frequer

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IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

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IEEE CNF IEEE Conference Proceeding

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[Monolithic Phase-Locked Loops and Clock Recovery Circuits](#)

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IEEE CNF IEEE Conference Proceeding

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Hwang-Cherng Chow; Yeh, N.-L.;
[Circuits and Systems, 2005. 48th Midwest Symposium on](#)
7-10 Aug. 2005 Page(s):1342 - 1345 Vol. 2
Digital Object Identifier 10.1109/MWSCAS.2005.1594358
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- ☐ 2. **A CMOS 10 Gb/s clock and data recovery circuit with a novel adjustable phase detector**
Xinyu Chen; Green, M.M.;
[Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International](#)
Volume 4, 23-26 May 2004 Page(s):IV - 301-4 Vol.4
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- ☐ 3. **A Si bipolar phase and frequency detector IC for clock extraction up to 8**
Pottbacker, A.; Langmann, U.; Schreiber, H.-U.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 27, Issue 12, Dec. 1992 Page(s):1747 - 1751
Digital Object Identifier 10.1109/4.173101
[AbstractPlus](#) | Full Text: [PDF](#)(552 KB) IEEE JNL
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- ☐ 4. **A 8 Gb/s Si bipolar phase and frequency detector IC for clock extraction**
Pottbacker, A.; Langmann, U.; Schreiber, H.-U.;
[Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSCC](#)
[International](#)
19-21 Feb. 1992 Page(s):162 - 163, 273
Digital Object Identifier 10.1109/ISSCC.1992.200427
[AbstractPlus](#) | Full Text: [PDF](#)(236 KB) IEEE CNF
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- ☐ 5. **Two Novel Phase-Frequency Detectors**
Kikkert, C.J.;
[Circuits and Systems, 2006. APCCAS 2006. IEEE Asia Pacific Conference on](#)
4-7 Dec. 2006 Page(s):712 - 715
Digital Object Identifier 10.1109/APCCAS.2006.342106
[AbstractPlus](#) | Full Text: [PDF](#)(484 KB) IEEE CNF
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- ☐ 6. **Noise analysis of phase-locked loops**
Mehrotra, A.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on
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Volume 49, Issue 9, Sep 2002 Page(s):1309 - 1316
Digital Object Identifier 10.1109/TCSI.2002.802347
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(338 KB\)](#) IEEE JNL
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- ☐ 7. **A 2.5-10-GHz clock multiplier unit with 0.22-ps RMS jitter in standard 0.18 CMOS**
van de Beek, R.C.H.; Vaucher, C.S.; Leenaerts, D.M.W.; Klumperink, E.A.M.; I
Solid-State Circuits, IEEE Journal of
Volume 39, Issue 11, Nov. 2004 Page(s):1862 - 1872
Digital Object Identifier 10.1109/JSSC.2004.835833
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1168 KB\)](#) IEEE JNL
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- ☐ 8. **Noise analysis of phase-locked loops**
Mehrotra, A.;
Computer Aided Design, 2000. ICCAD-2000. IEEE/ACM International Conference on
5-9 Nov. 2000 Page(s):277 - 282
Digital Object Identifier 10.1109/ICCAD.2000.896486
[AbstractPlus](#) | Full Text: [PDF\(600 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ 9. **Free false lock and timing recovery independent frequency detector**
Lozhkin, A.N.;
Communications, 1999. ICC '99. 1999 IEEE International Conference on
Volume 2, 6-10 June 1999 Page(s):1250 - 1255 vol.2
Digital Object Identifier 10.1109/ICC.1999.765521
[AbstractPlus](#) | Full Text: [PDF\(492 KB\)](#) IEEE CNF
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- ☐ 10. **A digitally controlled phase-locked loop with a digital phase-frequency detector acquisition**
In-Chul Hwang; Sang-Hun Song; Soo-Won Kim;
Solid-State Circuits, IEEE Journal of
Volume 36, Issue 10, Oct. 2001 Page(s):1574 - 1581
Digital Object Identifier 10.1109/4.953487
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- ☐ 11. **A wide-range power-efficient CMOS phase-locked loop with a differential programmable VCO**
Chen, R.Y.; Ming-Yu Hsieh; Peng-Min Peng;
Signals, Circuits and Systems, 2005. ISSCS 2005. International Symposium on
Volume 2, 14-15 July 2005 Page(s):673 - 676 Vol. 2
Digital Object Identifier 10.1109/ISSCS.2005.1511330
[AbstractPlus](#) | Full Text: [PDF\(252 KB\)](#) IEEE CNF
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- ☐ 12. **A low power and low noise frequency synthesizer with a integrated quad**
Seon-Ho Han; Yong-Sik Youn; Hyun-Kyu Yu; Mun-Yang Park;
Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE
8-10 June 2003 Page(s):307 - 310
[AbstractPlus](#) | Full Text: [PDF\(347 KB\)](#) IEEE CNF
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- ☐ 13. **A CMOS clock and data recovery with two-XOR phase-frequency detector**
Jin-Ku Kang; Dong-Hee Kim;
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on
Volume 4, 6-9 May 2001 Page(s):266 - 269 vol. 4

Digital Object Identifier 10.1109/ISCAS.2001.922223

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☐ **14. A dual-slope PFD/CP frequency synthesizer architecture with an adaptive algorithm**

Shuilong Huang; Zhihua Wang;
[Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on](#)
27-30 May 2007 Page(s):3924 - 3927
Digital Object Identifier 10.1109/ISCAS.2007.378658

[AbstractPlus](#) | Full Text: [PDF](#)(256 KB) IEEE CNF
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☐ **15. A fractional-n PLL frequency synthesizer design**

Seoncheol Kim; Youngsik Kim;
[SoutheastCon, 2005. Proceedings. IEEE](#)
8-10 April 2005 Page(s):84 - 87
Digital Object Identifier 10.1109/SECON.2005.1423222

[AbstractPlus](#) | Full Text: [PDF](#)(1856 KB) IEEE CNF
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☐ **16. A 1.7/spl sim/3.125Gbps clock and data recovery circuit using a gated fre**
Rong-Jyi Yang; Shen-luan Liu;

[Advanced System Integrated Circuits 2004. Proceedings of 2004 IEEE Asia-P.](#)
[on](#)
4-5 Aug. 2004 Page(s):326 - 329
Digital Object Identifier 10.1109/APASIC.2004.1349486

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☐ **17. Phase Locked Loop gain shaping for gigahertz operation**

Iniewski, K.; Magierowski, S.; Syrzycki, M.;
[Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International](#)
Volume 4, 23-26 May 2004 Page(s):IV - 157-60 Vol.4

[AbstractPlus](#) | Full Text: [PDF](#)(222 KB) IEEE CNF
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☐ **18. Phase frequency detectors for fast frequency acquisition in zero-dead-zo**
mobile communication systems

Kun-Seok Lee; Byeong-Ha Park; Han-il Lee; Min Jong Yoh;
[Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th](#)
16-18 Sept. 2003 Page(s):525 - 528.
Digital Object Identifier 10.1109/ESSCIRC.2003.1257188

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☐ **19. A 2.5 to 10GHz clock multiplier unit with 0.22ps RMS jitter in a 0.18/spl m**
technology

van de Beek, R.C.H.; Vaucher, C.S.; Leenaerts, D.M.W.; Pavlovic, N.; Mistry, I
E.A.M.; Nauta, B.;
[Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 20](#)
[International](#)
2003 Page(s):178 - 486 vol.1
Digital Object Identifier 10.1109/ISSCC.2003.1234256

[AbstractPlus](#) | Full Text: [PDF](#)(604 KB) | [Multimedia](#) IEEE CNF
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☐ **20. A low noise 9.95/10.66 GHz PLO for optical applications**

Gao, X.; Koechlin, M.; Lyons, C.; Chiesa, J.; Guven, G.; Katzin, P.;
[Microwave Symposium Digest, 2003 IEEE MTT-S International](#)
Volume 2, 8-13 June 2003 Page(s):729 - 732 vol.2

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- ☐ 21. **A 3.3 V high speed dual looped CMOS PLL with wide input locking range**
Hyuk-Jun Sung; Kwang Sub Yoon; Hong Ki Min;
Circuits and Systems, 1998. Proceedings. 1998 Midwest Symposium on
9-12 Aug. 1998 Page(s):476 - 479
Digital Object Identifier 10.1109/MWSCAS.1998.759534
[AbstractPlus](#) | Full Text: [PDF\(152 KB\)](#) IEEE CNF
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- ☐ 22. **A 200-Mbps/spl sim/2-Gbps continuous-rate clock-and-data-recovery circ**
Rong-Jyi Yang; Kuan-Hua Chao; Shen-luan Liu;
Circuits and Systems I: Regular Papers, IEEE Transactions on [see also Circu
Fundamental Theory and Applications, IEEE Transactions on]
Volume 53, Issue 4, April 2006 Page(s):842 - 847
Digital Object Identifier 10.1109/TCSI.2005.862071
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Messerschmitt, D.;
Communications, IEEE Transactions on [legacy, pre - 1988]
Volume 27, Issue 9, Sep 1979 Page(s):1288 - 1295
[AbstractPlus](#) | Full Text: [PDF\(656 KB\)](#) IEEE JNL
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- ☐ 24. **Clock and data recovery circuit with two exclusive-OR phase frequency c**
Dong-Hee Kim; Jin-Ku Kang;
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Volume 36, Issue 16, 3 Aug. 2000 Page(s):1347 - 1349
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- ☐ 25. **A /spl Delta//spl Sigma/ fractional-N frequency synthesizer with a multi-b:**
for 2.4 and 5GHz WLAN applications
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16-18 Sept. 2003 Page(s):651 - 654
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 Pottbacker, A.; Langmann, U.; Schreiber, H.-U.;
[Solid-State Circuits, IEEE Journal of](#)
 Volume 27, [Issue 12](#), Dec. 1992 Page(s):1747 - 1751
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- ☐ 3. **A 8 Gb/s Si bipolar phase and frequency detector IC for clock extraction**
 Pottbacker, A.; Langmann, U.; Schreiber, H.-U.;
[Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSC International](#)
 19-21 Feb. 1992 Page(s):162 - 163, 273
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[Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on](#)
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- ☐ 5. **A 2.5-10-GHz clock multiplier unit with 0.22-ps RMS jitter in standard 0.18 CMOS**
 van de Beek, R.C.H.; Vaucher, C.S.; Leenaerts, D.M.W.; Klumperink, E.A.M.;
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5-9 Nov. 2000 Page(s):277 - 282
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- ☐ **7. Free false lock and timing recovery independent frequency detector**
Lozhkin, A.N.;
Communications, 1999. ICC '99. 1999 IEEE International Conference on
Volume 2, 6-10-June 1999 Page(s):1250 - 1255 vol.2
Digital Object Identifier 10.1109/ICC.1999.765521
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In-Chul Hwang; Sang-Hun Song; Soo-Won Kim;
Solid-State Circuits, IEEE Journal of
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Digital Object Identifier 10.1109/4.953487
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Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE
8-10 June 2003 Page(s):307 - 310
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Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on
Volume 4, 6-9 May 2001 Page(s):266 - 269 vol. 4
Digital Object Identifier 10.1109/ISCAS.2001.922223
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- ☐ **11. A 1.7/spl sim/3.125Gbps clock and data recovery circuit using a gated frequency divider**
Rong-Jyi Yang; Shen-Iuan Liu;
Advanced System Integrated Circuits 2004. Proceedings of 2004 IEEE Asia-Pacific
4-5 Aug. 2004 Page(s):326 - 329
Digital Object Identifier 10.1109/APASIC.2004.1349486
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- ☐ **12. Phase Locked Loop gain shaping for gigahertz operation**
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- ☐ **13. Phase frequency detectors for fast frequency acquisition in zero-dead-zone mobile communication systems**
Kun-Seok Lee; Byeong-Ha Park; Han-il Lee; Min Jong Yoh;
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☐ **14. A 2.5 to 10GHz clock multiplier unit with 0.22ps RMS jitter in a 0.18/ μ m technology**

van de Beek, R.C.H.; Vaucher, C.S.; Leenaerts, D.M.W.; Pavlovic, N.; Mistry, I. E.A.M.; Nauta, B.;

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☐ **15. A low noise 9.95/10.66 GHz PLO for optical applications**

Gao, X.; Koechlin, M.; Lyons, C.; Chiesa, J.; Guven, G.; Katzin, P.;

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☐ **16. A 3.3 V high speed dual looped CMOS PLL with wide input locking range**

Hyuk-Jun Sung; Kwang Sub Yoon; Hong Ki Min;

[Circuits and Systems, 1998. Proceedings. 1998 Midwest Symposium on](#)

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☐ **17. Frequency Detectors for PLL Acquisition in Timing and Carrier Recovery**

Messerschmitt, D.;

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☐ **18. Clock and data recovery circuit with two exclusive-OR phase frequency c**

Dong-Hee Kim; Jin-Ku Kang;

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☐ **20. Low cost synthesised sources for VSAT frequency converter application**

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